Single CFTA Based Current-Mode Universal Biquad Filter

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Abstract: This paper introduces a new current-mode (CM) universal biquad filter structure with optimum number of active and passive elements. In the design, the proposed circuit uses a single active element namely, current follower trans-conductance amplifier (CFTA) and two grounded capacitors as passive elements. The main feature of the proposed circuit is that it can realize all five standard filtering functions such as low pass (LP), band pass (BP), high pass (HP), band stop (BS) and all pass (AP) responses across an explicit high impedance output terminal through the appropriate selection of three inputs. In addition, the same circuit is also capable to simultaneously realize three filtering functions (LP, BP and HP) by the use of single current input signal. Moreover, the proposed structure is suited for low voltage, low power operations and offers the feature of electronic tunability of pole-frequency and quality factor. Further to extend the utility of the proposed circuit block higher order current-mode filters are also realized through direct cascading. A detailed non-ideal and parasitic study is also included. The performance of the circuits has been examined using standard 0.25 µm CMOS parameters from TSMC.

Keywords: Analog signal processing, Biquad-filters, Current-mode, Tunable.

محاتب: أحادي ناقل للتوصلية تابع للتيار لمرشح الهوائيات العالمي معتمداً على حالة التيار

الملخص: تعرض هذه الورقة نمط تياري جديد للمرشح الكهربائي والذي يتم استخدامه في المنكات الامتثال للعناصر النشطة والخاملة. وفقاً للتصميم، فإن مجمع الدائرة الكهربائية يستخدم عنصر مفرد (مضخم ناقل تيار) مع محكشين كهربائيين. أن فائدة الدائرة المفردة تبدأ مع التيار المدخل الدائرة، والتي يمكن من خلالها تحقيق استجابة تمرير بطيئة، ومتعددة، وعالية، على التوالي، علاوة على ذلك، مع التيار الدائرة الثلاثية، فإنه يمكن أيضًا تحقيق جميع وظائف الترشيح الكهربائية بسهولة. يتضمن البناء المكرش الجهد المخفض، والعمليات المخفضة الطاقة، وتقدم ميزة قابلية التوليد الإلكترونية لقلب التردد وعامل الجدوى. بالإضافة إلى كونه مكرش، فإن الشحنات العالمية الرباطية تحقق من خلال التوصيل التعافي المباشر. لقد تم التفصيل احترامًا دراسة غير المقابلة والطويلة. وقد تم فحص أداء الدوائر الكهربائية باستخدام متغيرات معيار 0.25 ميرون.

المصطلحات المفتاحية: معالجة الإشارات الكهربائية، الفلاتر الهوائية، نمط تياري، قابلية التوليد

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1. Introduction

Analog circuit designers have paid a significant accent on the study and synthesis of current-mode (CM) continuous-time (CT) filter structures using variants of current conveyors suited for high performance analog signal processing applications (Toumazou et al. 1990; Kacar and Kuntman 2011). In the last few decades, circuit designers primarily focused on designing low cost, low supply voltage operable simple filter structures realizing all the standard filtering responses. These filter structures are termed as universal filters. Further, in the perspective of less chip area, cost reduction and lower average power consumption, the concluding remarks state that the circuit topology must be intended for an optimum use of active and passive elements in the biquad design (Satansup and Tangsrirat 2014). Another concern pertinent to the integrated circuit realization point of view is the electronic tuning aspects of filter parameters used for the fine adjustment of filter parameters against large manufacturing tolerances, which can also be used to compensate for deviations in the circuit performance parameters due to process tolerance, port parasitic, temperature drift, imperfections and aging etc. (Karybakas and Papazoglou 1999; Metin 2007). In the process, enormous papers on the synthesis of current-mode biquad filter circuits having one or more active elements are reported in the available literature (Keskin et al. 2006; Tomar et al. 2014a).

The circuits reported in references are capable of realizing all the five standard filtering functions in current-mode either simultaneously (Cicekoglu 2001; Maheshwari and Khan 2004; Maheshwari and Khan 2005) or one at a time (Singh et al. 2014; Tomar et al. 2014b; Singh et al. 2012) or both way (Wang et al. 2001) without changing the circuit structure. Beside it, most of the circuit structure except few (Cicekoglu 2001; Wang et al. 2001) is resister less and canonical. However, all these circuits require more than one active element to realize filtering functions. With a view to being adaptable towards the simplicity, low cost, lower power consumption and space saving of the circuits, it is beneficial to design the biquad filter by the use of single active element and minimum number of passive elements. Therefore, we have focused here only on the single active element based current-mode filters from the available literature (Arsian et al. 2006; Prasad et al. 2009) for the comparative purpose and hence, the detail features of all single active elements based current-mode biquad filters are compared and summarized in Table 1. Some of the circuits among the current-mode filters based on single active element as discussed in Table 1 are configured as single input three output (SITO) (Mangkalakeeree et al. 2009; Prasad et al. 2009) and remaining are configured as three input single output (TISO) (Arsian et al. 2006; Satansup et al. 2014). The SITO filters can realize at the most three filtering functions simultaneously whereas TISO filters can realize all five filtering functions but one function explicitly at a time. Unfortunately, most of the filter circuits (Arsian et al. 2006; Chang et al. 2007; Prasad et al. 2009; Tangsrirat 2010) and except (Satansup et al. 2012; Satansup et al. 2014) use at least three passive elements in the design.

Beside this, some of the circuit configurations also employ floating passive elements (Arsian et al. 2006; Biulek et al. 2009; Chang et al. 2007; Prasad et al. 2009; Sirirat et al. 2010; Singh et al. 2013; Tangsrirat 2010; Yuce et al. 2004) and, hence, are not favorable for IC implementation. Moreover, few circuits require inverted current input signals and/or component matching constraints (Arsian et al. 2006; Chang et al. 2007; Chaturvedi and Maheswari 2011; Prasad et al. 2009; Sirirat et al. 2010; Satansup et al. 2014) too for the filtering functions realization. Furthermore, none of the CM filters endorsed in Table 1 can be configured as single input multiple output (SIMO) as well as multiple input single output (MISO) simultaneously from the same structure and are inept to operate at low supply voltages with lower power consumption.

The current-mode filter structure proposed in this paper consists of single CFTA and two grounded capacitors and can realize LP, BP, HP, BS and AP filter functions in three input single output (TISO) and LP, BP, and HP filter functions in single input three output (SITO) configurations. The active element CFTA is slightly modified to get dual electronic tunability feature. The proposed structure is a resistor-less CMOS topology which neither requires inverted current input nor matching constraints for the realization of any filter function(s). With suitable impedance levels the proposed filter blocks are directly cascaded to obtain higher order filters (Kacar and Kuntman 2011; Tomar et al. 2014a). The proposed circuits are evaluated through P-SPICE programs on cadence tools using 0.25μm TSMC CMOS parameters (Prommee et al. 2009).
Table 1. Comparison among recent single active element based current-mode filters (Prasad et al. 2009; Arsian et al. 2006).

<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>(Prasad et al. 2009)</td>
<td>DOCDTA</td>
<td>SIMO</td>
<td>2R+2C</td>
<td>LP, BP, HP</td>
<td>2R</td>
<td>1 YES</td>
<td>NA</td>
<td>YES</td>
<td>NO</td>
<td>± 1 V</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>(Chaturvedi et al. 2011)</td>
<td>DVCC</td>
<td></td>
<td>2R+2C</td>
<td>LP, BP, HP</td>
<td>None</td>
<td>None</td>
<td>NO</td>
<td>9.7 MHz</td>
<td>YES</td>
<td>NO</td>
<td>± 2.5 V</td>
<td>4.9 mW</td>
</tr>
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<td>(Yuce et al. 2004)</td>
<td>CCII</td>
<td></td>
<td>2R+2C</td>
<td>LP, BP</td>
<td>1R</td>
<td>None</td>
<td>NO</td>
<td>1 MHz</td>
<td>NO</td>
<td>NO</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>(Herencsar et al. 2009)</td>
<td>CCTA</td>
<td></td>
<td>2R+2C</td>
<td>LP, BP, HP</td>
<td>None</td>
<td>1 YES</td>
<td>NA</td>
<td>159 KHz</td>
<td>NO</td>
<td>NO</td>
<td>± 3 V</td>
<td>NA</td>
</tr>
<tr>
<td>(Prasad et al. 2013)</td>
<td>VDTA</td>
<td>SIMO</td>
<td>1R+2C</td>
<td>LP, BP, HP</td>
<td>None</td>
<td>1 YES</td>
<td>NA</td>
<td>3 MHz</td>
<td>NO</td>
<td>NO</td>
<td>± 2 V</td>
<td>NA</td>
</tr>
<tr>
<td>(Singh et al. 2013)</td>
<td>MOCFTA</td>
<td></td>
<td>1R+2C</td>
<td>LP, BP, HP</td>
<td>1R</td>
<td>2 YES</td>
<td>NA</td>
<td>1 MHz</td>
<td>NO</td>
<td>NO</td>
<td>± 1.5 V</td>
<td>1.18 mW</td>
</tr>
<tr>
<td>(Kacar et al. 2012)</td>
<td>FDCCII</td>
<td></td>
<td>2R+2C</td>
<td>LP, BP, HP</td>
<td>None</td>
<td>2 YES</td>
<td>NO</td>
<td>10 MHz</td>
<td>NO</td>
<td>NO</td>
<td>± 1.3 V</td>
<td>NA</td>
</tr>
<tr>
<td>(Biolek et al. 2009)</td>
<td>CDTA</td>
<td></td>
<td>1R+2C</td>
<td>LP, BP, HP</td>
<td>1R</td>
<td>1 YES</td>
<td>NA</td>
<td>10 MHz</td>
<td>NO</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
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<tr>
<td>(Tangsrirat 2010)</td>
<td>CFTA</td>
<td></td>
<td>1R+2C</td>
<td>LP, BP, HP</td>
<td>1R</td>
<td>1 NO</td>
<td>NA</td>
<td>3.03 MHz</td>
<td>NO</td>
<td>NO</td>
<td>± 2 V</td>
<td>NA</td>
</tr>
<tr>
<td>(Satansup et al. 2012)</td>
<td>VDTA</td>
<td>SIMO</td>
<td>2C</td>
<td>LP, BP, HP</td>
<td>None</td>
<td>2 YES</td>
<td>NA</td>
<td>572 KHz</td>
<td>NO</td>
<td>NO</td>
<td>± 1.5 V</td>
<td>1.42 mW</td>
</tr>
<tr>
<td>(Mangkalakeeree et al. 2009)</td>
<td>CCCCTA</td>
<td></td>
<td>2C</td>
<td>LP, BP</td>
<td>None</td>
<td>1 YES</td>
<td>3 MHz</td>
<td>NO</td>
<td>YES</td>
<td>± 2 V</td>
<td>1 mW</td>
<td></td>
</tr>
<tr>
<td>(Satansup et al. 2014)</td>
<td>VDTA</td>
<td>MISO</td>
<td>1R+2C</td>
<td>LP, BP, HP, BS, AP</td>
<td>None</td>
<td>1 YES</td>
<td>1 MHz</td>
<td>YES</td>
<td>YES</td>
<td>± 1.65 V</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>(Chang et al. 2007)</td>
<td>CCCII</td>
<td></td>
<td>1R+2C</td>
<td>LP, BP, HP, BS, AP</td>
<td>1R</td>
<td>1 YES</td>
<td>1 MHz</td>
<td>YES</td>
<td>YES</td>
<td>± 3 V</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>(Kacar et al. 2012)</td>
<td>FDCCII</td>
<td></td>
<td>2R+2C</td>
<td>LP, BP, HP, BS, AP</td>
<td>None</td>
<td>1 YES</td>
<td>1.59 MHz</td>
<td>NO</td>
<td>NO</td>
<td>± 3 V</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>(Pandey and Paul 2011)</td>
<td>DVCCCTA</td>
<td></td>
<td>1R+2C</td>
<td>LP, BP, HP, BS, AP</td>
<td>None</td>
<td>None</td>
<td>NA</td>
<td>1.59 MHz</td>
<td>NO</td>
<td>NO</td>
<td>± 1.25 V</td>
<td>NA</td>
</tr>
<tr>
<td>(Sirirat et al. 2010)</td>
<td>CFTA</td>
<td></td>
<td>1R+2C</td>
<td>LP, BP, HP, BS, AP</td>
<td>1R</td>
<td>1 YES</td>
<td>1.12 MHz</td>
<td>YES</td>
<td>YES</td>
<td>± 3 V</td>
<td>NA</td>
<td></td>
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<tr>
<td>(Arsian et al. 2006)</td>
<td>CCII</td>
<td></td>
<td>2R+2C</td>
<td>LP, BP, HP, BS, AP</td>
<td>1C</td>
<td>1 YES</td>
<td>NA</td>
<td>8 MHz</td>
<td>NO</td>
<td>NO</td>
<td>± 0.75 V</td>
<td>0.6 mW</td>
</tr>
<tr>
<td>Proposed</td>
<td>CFTA</td>
<td>Both SIMO/MISO</td>
<td>2C</td>
<td>LP, BP, HP, BS, AP</td>
<td>None</td>
<td>None</td>
<td>YES</td>
<td>8 MHz</td>
<td>NO</td>
<td>NO</td>
<td>± 0.75 V</td>
<td>0.6 mW</td>
</tr>
</tbody>
</table>
2. Basics of CFTA

Since after its inception as current-mode active element and its terminal impedance suitability for current-mode analog signal processing applications, CFTA have been received considerable attention from the circuit designers (Satansup and Tangsirirat 2011; Tomar et al. 2014a; Singh et al. 2012; Singh and Maheswari 2013). The conventional CFTA can be further modified for additional advantage of dual electronic tunability. The modified CFTA with symbolic diagram is shown in Fig. 1 and can be described through the following set of equations

\[ V_r = V_{z1} = V_{z2} = V_{z3} \]

\[ I_r = I_{z1} = I_{z2} = I_{z3} = g_{m1} V_{z1} \]

\[ I_{x1} = g_{m2} V_{z2} \]

Realization of the modified CFTA using CMOS is depicted in Fig. 2. The transconductance parameters \( g_{m1} \) and \( g_{m2} \) of the CMOS implemented CFTA (Tomar et al. 2014b; Singh et al. 2012) can be related with the biasing currents \( I_{S1} \) and \( I_{S2} \), respectively as:

\[ g_{m1} = \beta I_{S1} \quad \text{and} \quad g_{m2} = \beta I_{S2} \]

Where, \( \beta = \mu_0 C_{OX} (W/L) \) is the process parameter of NMOS transistors M8-M9, M15-M16 forming differential pairs at the transconductance stages of employed CFTA.

3. Proposed Current-Mode Filter

The proposed current-mode biquad filter circuit as shown in Fig. 3 employs single CFTA as the active element and two grounded capacitors. The use of grounded capacitors is elegant for integrability (Bhusan and Newcomb 1967). The proposed circuit in Fig. 3 can be configured as either three input single output or single input three output configurations through appropriate selection of input and output current signal(s). The workability of the proposed current-mode filter structure can be described in following two different cases:

3.1 Case-I: TISO Filter Configuration

If the proposed circuit in Fig. 3 is analyzed with three current input signals \( (I_{in1}, I_{in2}, I_{in3}) \), the expression for current output \( (I_{out}) \) can be obtained as:

\[ I_{out} = \frac{-C_2 s^2 I_{in1} - g_{m1} g_{m2} I_{in2} + C_2 s^2 + g_{m1} + g_{m2} I_{in3}}{D(s)} \]

Where, \( D(s) = s^2 C_2 + g_{m1} C_1 + g_{m2} \)

![Figure 1. Schematic symbol of modified CFTA.](image)

![Figure 2. CMOS implementation of CFTA.](image)
It can be easily retrieved from equation (3) that different CM filtering responses can be obtained at current output \( I_{\text{out}} \) by selecting current inputs appropriately, as follows:

- For \( I_{\text{in}1} = I_{\text{in}2} = I_{\text{in}3} = I_{\text{in}} \) a non-inverted LP response is obtained.
- For \( I_{\text{in}1} = I_{\text{in}} \) and \( I_{\text{in}2} = I_{\text{in}3} = 0 \) an inverted HP response is obtained.
- For \( I_{\text{in}2} = I_{\text{in}} \) and \( I_{\text{in}1} = I_{\text{in}3} = 0 \) an inverted BP response is obtained.
- For \( I_{\text{in}2} = I_{\text{in}3} = I_{\text{in}} \) and \( I_{\text{in}1} = 0 \) a non-inverted BS response is obtained.
- For \( I_{\text{in}2} = 2I_{\text{in}}, I_{\text{in}3} = I_{\text{in}} \) and \( I_{\text{in}1} = 0 \) a non-inverted AP response is obtained.

### 3.2 Case-II: SITO Configuration

With single current input \( (I_{\text{in2}} = I_{\text{in}}) \), the proposed circuit in Fig. 3 is capable to realize LP, BP and HP responses, simultaneously across three different current outputs \( I_{\text{LP}}, I_{\text{BP}}, I_{\text{HP}} \). The transfer functions for received filtering responses are as follows:

\[
\frac{I_{\text{BP}}}{I_{\text{in}}} = -g_{m2} C_1 s \frac{D(s)}{D(s)} \tag{5}
\]

\[
\frac{I_{\text{LP}}}{I_{\text{in}}} = g_{m1} g_{m2} \frac{C_1 s}{D(s)} \tag{6}
\]

\[
\frac{I_{\text{HP}}}{I_{\text{in}}} = C_1 C_2 s^2 \frac{D(s)}{D(s)} \tag{7}
\]

From cases I and II, it can be remarked that proposed circuit in Fig. 3 can realize all the standard filter functions (LP, BP, HP, BS, and AP) across an explicit high impedance current output terminal by the appropriate selection of three current input signals. In addition, the same structure realizes LP, BP, HP responses, simultaneously by the use of single current input signal. Thus, the proposed circuit can be used as either TISO or SITO current-mode biquad filter without changing the structure and neither requires any component matching constraint nor inverted current input signal for any of the response realization.

The filter’s characteristic parameters like pole frequency \( \omega \), quality factor \( Q \) and bandwidth \( BW \) can be derived from the transfer function as:

\[
\omega = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}}, \quad Q = \sqrt{\frac{C_1 g_{m1} g_{m2}}{C_2}}, \quad BW = \frac{g_{m2}}{C_2} \tag{8}
\]

On substituting trans-conductance parameters \( g_{m1} \) and \( g_{m2} \) from equation (2) we find that equation (8) turns out to be:

\[
\omega = \sqrt{\frac{\beta_s (I_{S1} I_{S2})^{1/2}}{C_1 C_2}}, \quad Q = \sqrt{\frac{C_1}{C_2}} \left( \frac{I_{S1}}{I_{S2}} \right)^{1/2} \tag{9}
\]

From equation (9), it is evident that the pole frequency can be tuned precisely, without distressing quality factor, if the ratio of biasing currents \( I_{S1} \) and \( I_{S2} \) is kept to be constant. The bandwidth \( BW \) of the proposed filter circuit can also be expressed as:

\[
BW = \frac{(\beta_s I_{S2})^{1/2}}{C_2} \tag{10}
\]

Equation (10) shows that the \( BW \) can solely be controlled by only biasing current \( I_{S2} \). From equations (9) and (10), it is clearly seen that filter’s parameters \( \omega \) and \( Q \) can be electronically adjusted by regulating the only biasing current \( I_{S1} \) without influencing \( BW \).

### 4. Non-ideal and Parasitic Effects

#### 4.1 Non-Ideal Analysis

This section describes the non-ideal aspects of the proposed biquad structure. For this a non-ideal CFTA can be modeled through modified set of equations, as follows:
\[ V_I = 0, I_{Z1} = I_{Z2} = I_{Z3} = \alpha I_f, I_{\pm Z1} = \gamma_1 I_m I_{Z1}, \]
\[ I_{\pm Z2} = \gamma_2 I_m I_{Z2} \quad (11) \]

Where, \( \alpha = 1 - \epsilon \) with \( |\epsilon| << 1 \) represents the current tracking errors between \( f \) to \( Z_i \) (\( i = 1, 2, 3 \)) terminals of CFTA and depends on the ratio of PMOS trans-conductance. With the use of identical PMOS transistors at the input stage, \( \alpha \) may approach to unity. Similarly, \( \gamma_1 \) and \( \gamma_2 \) are the trans-conductance inaccuracies between \( Z_1 \) to \( \pm X_1 \) and \( Z_2 \) to \( \pm X_2 \) terminals, respectively. On considering these non-ideal factors of the CFTA and re-analyzing the proposed filter of Fig. 3, we get the similar denominator for each current output expressions as:

\[ D(s) = s^2 C_1 C_2 + \gamma_2 g_m s_1 C_1 s + \gamma_2 g_m s_2 C_1 s \quad (12) \]

With involved non-idealities, the modified \( \omega \) and \( Q \) are obtained from equation (12) as:

\[ \omega = \sqrt{\frac{\gamma_2 g_m s_1 C_1 s}{C_1 C_2}}, \quad Q = \sqrt{\frac{\gamma_2 g_m s_2 C_1 s}{\gamma_2 C_1 s}} \quad (13) \]

From equation (13), it can be seen that minor deviations may occur in \( \omega \) and \( Q \) due to involved non-ideal factors. Though these slight deviations can be ignored as non-ideal factors \( \alpha \), \( \gamma_1 \) and \( \gamma_2 \) are immum to one at operational frequency. However, to what an extent the filter’s characteristic may actually be deviated due to possible changes in the design can be visualized by sensitivity coefficients which are as follows:

\[ S_{\gamma_1, \gamma_2, g_m, s_2}^{C_1, C_2} = \frac{1}{2}, \quad S_{C_1, C_2}^{\omega} = -\frac{1}{2} \quad (14) \]
\[ S_{\gamma_1, \gamma_2, g_m}^{s_1, s_2} = \frac{1}{2}, \quad S_{\gamma_1, \gamma_2, g_m}^{0} = -\frac{1}{2} \quad (15) \]

Hence, we can state that the entire sensitivity coefficients are within ‘half’ in magnitude.

### 4.2 Parasitic Effects

In this section, the performance of the proposed current-mode filter circuit in the presence of diverse parasitic impedance effects of the CFTA are to be considered. A practical CFTA, similar to any other active including various ports parasitic is shown in Fig. 4. These are port \( Z_1, Z_2 \) and \( Z_3 \) parasitic in the form of \( R_{Z1} / / C_{Z1}, R_{Z2} / / C_{Z2} \) and \( R_{Z3} / / C_{Z3} \) respectively, and ports \( X_1, X_2 \) parasitic in the form of \( R_{X1} / / C_{X1}, R_{X2} / / C_{X2} \) and port \( f \) parasitic in the form of \( R_{f} \). In Fig. 4 the \( X_2 \) port parasitic \( R_{X2} \) and \( C_{X2} \) appear between the high impedance terminal and ground. To abolish their effect, the CFTA should be well designed to comprise a very low port parasitic \( R_{f} \). Ideally, the value of \( R_{f} \) is zero and terminal \( f \) is virtually grounded.

Since these parasitic impedances are connected between true ground and virtual ground, these are, therefore, almost ineffective (Singh et al. 2012). The external capacitances \( C_1 \) and \( C_2 \) can be chosen to be much greater than the parasitic capacitances at the \( Z_1, Z_2 \), \( X_1 \) and \( X_2 \) terminals of CFTA i.e. \( C_1, C_2 >> C_{Z1}, C_{Z2}, C_{X1}, C_{X2} \).

![Figure 4. Modified CFTA with port parasitic.](image)

To visualize the effects of various parasitic impedances on the performance of the proposed current-mode filter circuit, the proposed circuit is reanalyzed in the presence of various ports parasitic of CFTA. For this purpose, current-mode BP response is taken into consideration. By taking the above discussion and parasitic effects into account and on further reanalyzing the proposed current-mode filter, we get the following expression for the BP filter at \( I_{out} \).

\[ I_{BP} = \frac{g_m^2}{C_2} \left( \frac{s + \frac{1}{C_2 R_{Z1}}}{s^2 + s \frac{g_m^2}{C_2} + \frac{g_m^2 M}{C_2 C_1}} \right) \quad (16) \]

Where, \( L = 1 + \frac{1}{g_m R_C} \) and \( M = 1 + \frac{1}{g_m R_{Z1}} \) (17)

\[ I_m = \frac{C_2}{1 + \frac{1}{g_m R_{Z1}}} \] (18)

With, \( R_C = R_{Z2} / / R_{X1} \) (19)

And hence, filter parameters in equations (8) to (10) are changed to:
By considering $C_1=C_2$, and $g_{m1}=g_{m2}$ in the yielded due to various ports parasitic of CFTA. In equations (16)-(22), undesirable factors are as and passive components value were determined with $f = 8 \text{ MHz}$ at designed to realize biquadratic characteristics and response, if we choose the design criterion given proposed filter may approach towards ideal eliminated or minimized and hence, the design, these undesirable factors can be shown in Fig. 2. The dimensions of MOS technology (TSMC 0.25µm process parameters) as Fig. 1 was implemented using standard CMOS employed CFTA as given in programs to authenticate the theoretical expectations. The employed CFTA as given in Fig. 1 was implemented using standard CMOS technology (TSMC 0.25µm process parameters) as shown in Fig. 2. The dimensions of MOS transistors were obtained as summarized in Table 2. The circuit was biased with power supply $V_{DD} = -V_{SS} = 0.75 \text{V}$ and $V_{BB} = -0.32 \text{V}$ and having varying frequency from 50 KHz to 900 KHz.

It can be observed that the THD figures are adequate and not more than 3%, causes the output signal is not distorted significantly for an applied input signal of varying frequency as shown in Fig. 11. To observe the effect of passive component mismatching on the filter’s performance, Monte-Carlo analysis has been performed for 100 samples.

For this, the BP filter of SITO configuration is also shown in Fig. 8, which was obtained by maintaining the product of $I_{S1}$ and $I_{S2}$ to be a constant as $(I_{S1} = 10 \mu \text{A}, I_{S2} = 160 \mu \text{A})$, $(I_{S1} = 16 \mu \text{A}, I_{S2} = 100 \mu \text{A})$, $(I_{S1} = 32 \mu \text{A}, I_{S2} = 50 \mu \text{A})$, and $(I_{S1} = 64 \mu \text{A}, I_{S2} = 25 \mu \text{A})$ respectively.

In Fig. 9, the time-domain analysis of BP filter (SITO configuration) is displayed, which was obtained by applying a sinusoidal input of $80 \mu \text{A}$ peak to peak at 7.94 MHz. Similarly, the time-domain analysis of LP filtering function (TISO configuration) is also shown in Fig. 10, which was obtained by applying a sinusoidal input of $80 \mu \text{A}$ peak to peak at 200 MHz. Next, the THDs of the LP response of the proposed circuit were also measured by applying a current input sinusoidal signal of peak amplitude of $40 \mu \text{A}$ and having varying frequency from 50 KHz to 900 KHz.

For different filtering responses the pole frequency was measured as 7.94 MHz, which deviated only by 0.75% from the numerical designed value of 8 MHz. To show the electronic tuning aspects of the proposed current-mode filter, the circuit is further simulated to obtain various BP responses at different sets of $I_{S1}$ and $I_{S2}$ in such a way so that $I_{S1} = I_{S2} = 5 \mu \text{A}, 10 \mu \text{A}, 30 \mu \text{A}, 150 \mu \text{A}$, which result in to the pole frequency variation as 1.25 MHz, 3.22 MHz, 7.25 MHz and 12.03 MHz, respectively, at constant $Q = 1$. The simulated result showing the pole frequency tuning aspect independent of $Q$ is shown in Fig. 7. Similarly, the simulation results showing the tuning feature of $Q$ independent of $I_{B}$ for the SITO configuration is also shown in Fig. 8, which were obtained by maintaining the product of $I_{S1}$ and $I_{S2}$ to be a constant as $(I_{S1} = 10 \mu \text{A}, I_{S2} = 160 \mu \text{A})$, $(I_{S1} = 16 \mu \text{A}, I_{S2} = 100 \mu \text{A})$, $(I_{S1} = 32 \mu \text{A}, I_{S2} = 50 \mu \text{A})$, and $(I_{S1} = 64 \mu \text{A}, I_{S2} = 25 \mu \text{A})$ respectively.

In this section, the current-mode universal filter in Fig. 3 has been simulated using PSPICE programs to authenticate the theoretical expectations. The employed CFTA as given in Fig. 1 was implemented using standard CMOS technology (TSMC 0.25µm process parameters) as shown in Fig. 2. The dimensions of MOS transistors were obtained as summarized in Table 2. The circuit was biased with power supply $V_{DD} = -V_{SS} = 0.75 \text{V}$ and $V_{BB} = -0.32 \text{V}$ and designed to realize biquadratic characteristics with $f = 8 \text{ MHz}$ at $Q = 1$. In design, the active and passive components value were determined as $I_{S1} = I_{S2} = 40 \mu \text{A}$ and $C_1 = C_2 = 10 \text{ pF}$, which resulted in total average power consumption of about 0.6 mW. Fig. 5 shows the simulated and ideal current-gain responses of BP, LP and HP filter functions for the SITO configuration of the proposed current-mode filter circuit. Similarly, for the TISO configuration the simulated and ideal current-gain and phase responses for LP, HP, BP, BS and AP filtering functions are shown in Fig. 6. In Fig. 5 and Fig. 6 the difference between ideal and simulated results is clearly visible along with distortion (spike) beyond 670 MHz or so. Which is obviously due to involved non ideal factors and parasitic effects dominating at higher frequencies. However, at working frequencies these non ideal factors were found to be unified as discussed in section

$$\omega^* = \omega \sqrt{M}$$

$$\left(\frac{\omega}{Q}\right)^* = \frac{g_{m2}}{C_2} \left[ L \right] = \frac{\omega}{Q} \left[ L \right]$$

and

$$Q^* = \frac{g_{m2} C_2 \sqrt{M}}{g_{m2} C_1} = Q \left[ \frac{\sqrt{M}}{L} \right]$$

In equations (16)-(22), undesirable factors are yielded due to various ports parasitic of CFTA. By considering $C_1=C_2$, and $g_{m1}=g_{m2}$ in the design, these undesirable factors can be eliminated or minimized and hence, the proposed filter may approach towards ideal response, if we choose the design criterion given in equation (23).

$$\frac{1}{g_{m2} R_{Z1}} << 1, \quad \frac{1}{g_{m2} R_C} << 1, \quad |\omega C_1| >> \frac{1}{R_{Z1}}$$

5. Simulation Results

Table 2. The circuit was biased with power supply $V_{DD} = -V_{SS} = 0.75 \text{V}$ and $V_{BB} = -0.32 \text{V}$ and designed to realize biquadratic characteristics with $f = 8 \text{ MHz}$ at $Q = 1$. In design, the active and passive components value were determined as $I_{S1} = I_{S2} = 40 \mu \text{A}$ and $C_1 = C_2 = 10 \text{ pF}$, which resulted in total average power consumption of about 0.6 mW. Fig. 5 shows the simulated and ideal current-gain responses of BP, LP and HP filter functions for the SITO configuration of the proposed current-mode filter circuit. Similarly, for the TISO configuration the simulated and ideal current-gain and phase responses for LP, HP, BP, BS and AP filtering functions are shown in Fig. 6. In Fig. 5 and Fig. 6 the difference between ideal and simulated results is clearly visible along with distortion (spike) beyond 670 MHz or so. Which is obviously due to involved non ideal factors and parasitic effects dominating at higher frequencies. However, at working frequencies these non ideal factors were found to be unified as discussed in section

4. For different filtering responses the pole frequency was measured as 7.94 MHz, which deviated only by 0.75% from the numerical designed value of 8 MHz.

The employed CFTA as given in Fig. 1 was implemented using standard CMOS technology (TSMC 0.25µm process parameters) as shown in Fig. 2. The dimensions of MOS transistors were obtained as summarized in Table 2. The circuit was biased with power supply $V_{DD} = -V_{SS} = 0.75 \text{V}$ and $V_{BB} = -0.32 \text{V}$ and designed to realize biquadratic characteristics with $f = 8 \text{ MHz}$ at $Q = 1$. In design, the active and passive components value were determined as $I_{S1} = I_{S2} = 40 \mu \text{A}$ and $C_1 = C_2 = 10 \text{ pF}$, which resulted in total average power consumption of about 0.6 mW. Fig. 5 shows the simulated and ideal current-gain responses of BP, LP and HP filter functions for the SITO configuration of the proposed current-mode filter circuit. Similarly, for the TISO configuration the simulated and ideal current-gain and phase responses for LP, HP, BP, BS and AP filtering functions are shown in Fig. 6. In Fig. 5 and Fig. 6 the difference between ideal and simulated results is clearly visible along with distortion (spike) beyond 670 MHz or so. Which is obviously due to involved non ideal factors and parasitic effects dominating at higher frequencies. However, at working frequencies these non ideal factors were found to be unified as discussed in section

$$\omega^* = \omega \sqrt{M}$$

$$\left(\frac{\omega}{Q}\right)^* = \frac{g_{m2}}{C_2} \left[ L \right] = \frac{\omega}{Q} \left[ L \right]$$

and

$$Q^* = \frac{g_{m2} C_2 \sqrt{M}}{g_{m2} C_1} = Q \left[ \frac{\sqrt{M}}{L} \right]$$

In equations (16)-(22), undesirable factors are yielded due to various ports parasitic of CFTA. By considering $C_1=C_2$, and $g_{m1}=g_{m2}$ in the design, these undesirable factors can be eliminated or minimized and hence, the proposed filter may approach towards ideal response, if we choose the design criterion given in equation (23).

$$\frac{1}{g_{m2} R_{Z1}} << 1, \quad \frac{1}{g_{m2} R_C} << 1, \quad |\omega C_1| >> \frac{1}{R_{Z1}}$$
Figure 5. Current-gain responses of LP, HP and BP filters for SITO configuration of the proposed filter in Figure 3.
Figure 6. Simulated and Ideal Current-gain and phase responses for TISO configuration of the proposed filter in Figure 3 (a) LP (b) HP (c) BP (d) BS and (e) AP filter functions.

Figure 7. Simulated BP responses of SITO configuration of the proposed filter in Figure 3, showing variation in pole frequency, and keeping Q = 1.
Figure 8. Simulated BP responses of SITO configuration showing variation in $Q$, by keeping pole frequency at 7.94 MHz.

Figure 9. Time domain response for BP filter of SITO configuration of the proposed filter in Figure 3.

Figure 10. Time domain response for LP filter of TISO configuration of the proposed filter in Figure 3.
6. Application: Higher Order Filters

To further support the proposed CM filter topology in Fig. 3, it is used as a general purpose structure for realizing higher order current-mode filter (Kacar and Kuntman 2011; Tomar et al. 2014a). For example, nth order (where n = even) BP filter and HP filter are shown in Fig. 13 and Fig. 14, which are implemented through direct cascading (Maheshwari et al. 2004) of m = n/2, similar proposed blocks without using any impedance matching or coupling. Direct cascading facilitates with no lower cut-off frequency limitations and circuit can operate from low to High frequency range.

Simulations are next performed for the 4th, 6th and 8th order fourth-order filter to illustrate the frequency domain performance of the circuit and corresponding results are shown in Fig. 15 and Fig. 16. In this design, the component values for each of the filter block (1, 2,...,m) were chosen as Ism = 40 µA and C1m = C2m = 10 pF. The voltage supply rails were used as VDD = -VSS = 0.75 V with a bias VBB = -0.32 V. From different simulation results, it is evident that the higher order circuits realized through direct cascading are attractive choice and operated efficiently at low supply rails with least power consumption.
Figure 13. $N^{th}$-order band pass (BP) filter, derived through direct cascading of the proposed circuit blocks in Figure 3.

Figure 14. $N^{th}$-order high pass (HP) filter, derived through direct cascading of the proposed circuit blocks in Figure 3.

Table 2. Dimensions of MOS transistors in Figure 2.

<table>
<thead>
<tr>
<th>MOS Transistors</th>
<th>Dimensions W (μm)/L (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1$, $M_2$</td>
<td>1/0.25</td>
</tr>
<tr>
<td>$M_3$-$M_7$, $M_{10}$-$M_{14}$, $M_{17}$-$M_{21}$</td>
<td>3/0.25</td>
</tr>
<tr>
<td>$M_8$, $M_9$, $M_{15}$, $M_{16}$</td>
<td>15/0.25</td>
</tr>
<tr>
<td>$M_{22}$-$M_{27}$, $M_{32}$-$M_{33}$, $M_{35}$-$M_{41}$</td>
<td>5/0.25</td>
</tr>
<tr>
<td>$M_{41}$</td>
<td></td>
</tr>
<tr>
<td>$M_{24}$</td>
<td>10/0.25</td>
</tr>
<tr>
<td>$M_{26}$, $M_{34}$</td>
<td>4.2/0.25</td>
</tr>
</tbody>
</table>
Figure 15. Current-gain and corresponding phase response for the \(N\)th-order (\(N = 2, 4, 6, 8\)) BP response of Figure 13.

Figure 16. Current-gain and corresponding phase response for the \(N\)th-order (\(N = 2, 4, 6, 8\)), HP response of Figure 14.
7. Conclusion

In this paper, a single CFTA and two grounded capacitors based current-mode biquad filter is proposed and verified using simulation results. In addition, non ideal aspects and parasitic impedance effects of the CFTA were also considered in details. The simulation results agree quite well with the theoretical expectations.

The proposed circuit has a number of noticeable advantages as discussed below. The proposed circuit shows versatility by realizing LP, BP, HP, BS and AP functions in TISO as well as LP, BP, HP responses as the SITO configuration. The use of a single active element makes the circuit topology simpler. Moreover, the use of two grounded capacitors provides a canonical structure, leads to the option for integrated circuit implementation and for parasitic reduction. Moreover, the circuit neither requires inverted current input(s) nor any component matching conditions for response realization, and thus eliminates the need of complex external circuitry. Orthogonal control of Q and \( \omega \) via biasing currents suited for practical adjustments in music and speech synthesis. The proposed circuit is a low voltage and low power structure, hence it is suited for battery operated systems. Expansion possibility of the proposed circuit for higher order realization through direct cascading validates its usefulness for analog signal processing. The CMOS compatibility of the circuit is fully suited for low cost integrated circuit implementation. Moreover, the circuit offer low active and passive sensitivity performance.

A careful inspection of Table 1 and introductory section of this study describes the superiority of the proposed filter block over other single active element based designs and finally concludes that none of the earlier reported current-mode filters offers all the above described features simultaneously.

References


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