NEW ASYMMETRIC 21-LEVEL INVERTER WITH REDUCED NUMBER OF SWITCHES

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ABSTRACT: Multilevel inverter plays an important role in the field of modern power electronics and is widely being used for many high voltage and high power industrial and commercial applications. The objective of this paper is to design and simulate the modified asymmetric multilevel inverter topology with reduced number of switches. The proposed inverter topology synthesizes 21-level output voltage during symmetric operation using three DC voltage sources and twelve switches 8 main switches and 4 auxiliary switches. The different methods of calculating the switching angles are presented in this paper. The MATLAB/Simulink software is used to simulate the proposed inverter. The performance of the proposed inverter is analyzed and the corresponding simulation results are presented in this paper.

محول جديد غير متماثل ذو 21 مستوى مع عدد مفاتيح أقل

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الملخص: يلعب المحول متعدد المستويات دورًا مهمًا في مجال الإلكترونيات الحديثة للطاقة ويستخدم على نطاق واسع في العديد من التطبيقات الصناعية والتجارية ذات الجهد العالي وكذلك تلك المتطلبة طاقة فائقة. إن الهدف من هذه الورقة البحثية هو تصميم ومحاكاة طوبولوجيا المحول المعدل وغير المتماثل و المتعدد المستويات مع تقليل عدد المفاتيح. وتعمل طوبولوجيا المحول المقترحة على تجميع الجهد الخارج ذو المستويات الـ 21 أثناء عملية التشغيل المتماثلة باستخدام ثلاثة مصادر جهد لتيار مباشر و اثني عشر مفتاحا (8 مفاتيح رئيسية و 4 مفاتيح مساعدة). ويقدم الباحثان الطرق المختلفة لحساب زوايا التبديل في هذه الورقة البحثية. كما يقوما باستخدام برمجيات ماتلاب/سيمالينك لمحاكاة المحول المقترح. ويقومان في هذه الورقة بتحليل أداء المحول المقترح وعرض نتائج المحاكاة المتشابهة.

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1. INTRODUCTION

To date multilevel inverters have greatly attracted many researchers due to their promising advantages for many industrial applications Meynard *et al.* (2002). The different advantages of multilevel inverters include lower switching frequency, lower switching losses, lower peak inverse voltage, smaller common mode voltage, lower harmonic distortion, less electromagnetic interference and high voltage capability Farakhor *et al.* (2015). The three main conventional multilevel inverter topologies are diode clamped or neutral point clamped (Busquets-Monge *et al.* 2008; Nabae *et al.* 1981), flying capacitor (Sadigh *et al.* 2010; Dargahi *et al.* 2014) and cascaded H-bridge with independent DC sources (Babaei *et al.* 2012; Babaei *et al.* 2015; Ramani *et al.* 2015). A high power rating can be achieved by the multilevel inverter. Various resources such as photovoltaic, battery and fuel cells can be used as a DC source, which can be easily interfaced for a high power and medium voltage application. In diode clamped inverter, large numbers of clamping diodes are required and regulating the capacitor voltages makes the control method more complex (Busquets-Monge *et al.* 2008; Nabae *et al.* 1981). In flying capacitor inverter, the size of the inverter is increased because of the requirement of more capacitors to achieve higher levels (Sadigh *et al.* 2010; Dargahi *et al.* 2014). Cascaded H-bridge inverter is more modular compared with other topologies. It can be easily expandable for a greater number of output voltage levels. However, to achieve higher output voltage levels, it requires a greater number of individual DC voltage sources for each module and semiconductor devices which increase the number gate drive circuit (Banaei *et al.* 2013; Toupchi Khosroshahi, 2014; Babaei *et al.* 2007; Prabaharan *et al.* 2015). To overcome these drawbacks, different topologies of multilevel inverters and modified pulse width modulation (PWM) methods have been developed in recent years. The PWM methods for multilevel inverters help to achieve the following objectives: easy implementation, reduced switching loss and minimum total harmonic distortion Grahame *et al.* (2003). The most widely used PWM techniques for multilevel inverters are the carrier based PWM techniques (Rahim *et al.* 2010; Jayabalan *et al.* 2017), selective harmonic elimination PWM (SHE-PWM) techniques Zhang *et al.* (2009) and the space vector based PWM techniques Vafakhah *et al.* (2010). Different topologies of transformer with less inverter are proposed to improve the efficiency and reduce current leakage (Thiyagarajan *et al.* 2016; Li *et al.* 2015; Islam *et al.* 2015). Lately, different topologies of multilevel inverters with reduced components have been developed (Karasani *et al.* 2016; Alishah *et al.* 2014; Samadaei *et al.* 2016; Babaei *et al.* 2014). These inverter topologies may be symmetric or asymmetric. However, these topologies do not considerably reduce the power switches. Hence, a new topology with reduced number of switching devices and voltage sources is proposed in this paper. Unlike the previously mentioned topologies, the proposed inverter topology reduces the total number of switches in the conduction path, thereby minimizes the switching losses.

In this paper, a modified multilevel asymmetric inverter topology with a reduced number of power switches is proposed. The proposed inverter uses three DC voltage sources and twelve switches (8 main switches and 4 auxiliary switches) to generate 21-level output voltage during asymmetric mode of operation. The different modes of operation of the proposed 21-level inverter are explained in Section-2. Section-3 presents the comparison of the proposed topology with the other existing topologies. Section-4 discusses the different methods of calculating the switching angles. The simulation results obtained using MATLAB/Simulink are explained in Section-5. The detailed conclusion is presented in Section-6.

2. PROPOSED INVERTER TOPOLOGY

Figure 1 shows the circuit diagram of the proposed 21-level asymmetric inverter. The proposed inverter consists of 3 DC voltage sources, 8 main switches and 4 auxiliary. Here, the switches S_4 and S_5 are bidirectional and other switches are unidirectional.

The term "asymmetric" is used as magnitude since the magnitude of each DC voltage sources is different. The proposed asymmetric multilevel inverter consists of two units, namely, a level creator unit and a polarity changing unit. The level creator unit creates ten levels of positive voltage. The polarity changing unit helps to change the polarity of the voltage generated by the level creator unit. The positive levels of voltage are obtained when the switches S_9 and S_{12} are turned ON and switches S_{10} and S_{11} are turned OFF. Similarly, the negative levels of voltage are obtained with the switches S_9 and S_{12} are turned OFF and switches S_{10} and S_{11} are turned ON. The proposed inverter can generate 21-level output voltage (*i.e.* 10 positive levels, 10 negative levels and 1 zero). In mode-1, S_1 and S_8 are
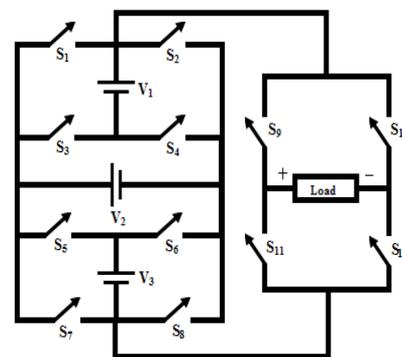

Figure 1. Proposed 21-level Inverter.

turned ON to get level-1 voltage. To get level-2 voltage during mode-2, the switches S_4 and S_7 are tuned ON. The level-3 voltage is obtained during mode-3 where the switches S_3 and S_7 are turned ON. During mode-4 operation, the switches S_3 and S_8 are tuned ON and the level-4 voltage is obtained. The level-5 voltage is obtained during mode-5 operation. During mode-5, the switches S_2 and S_5 are ON. During mode-6, the level-6 voltage is obtained with the switches S_1 and S_5 are ON.

(a) V_2

(b) V_1+V_2

(c) V_3-V_2

(d) $V_1+V_2+V_3$

(e) $- (V_1-V_2)$

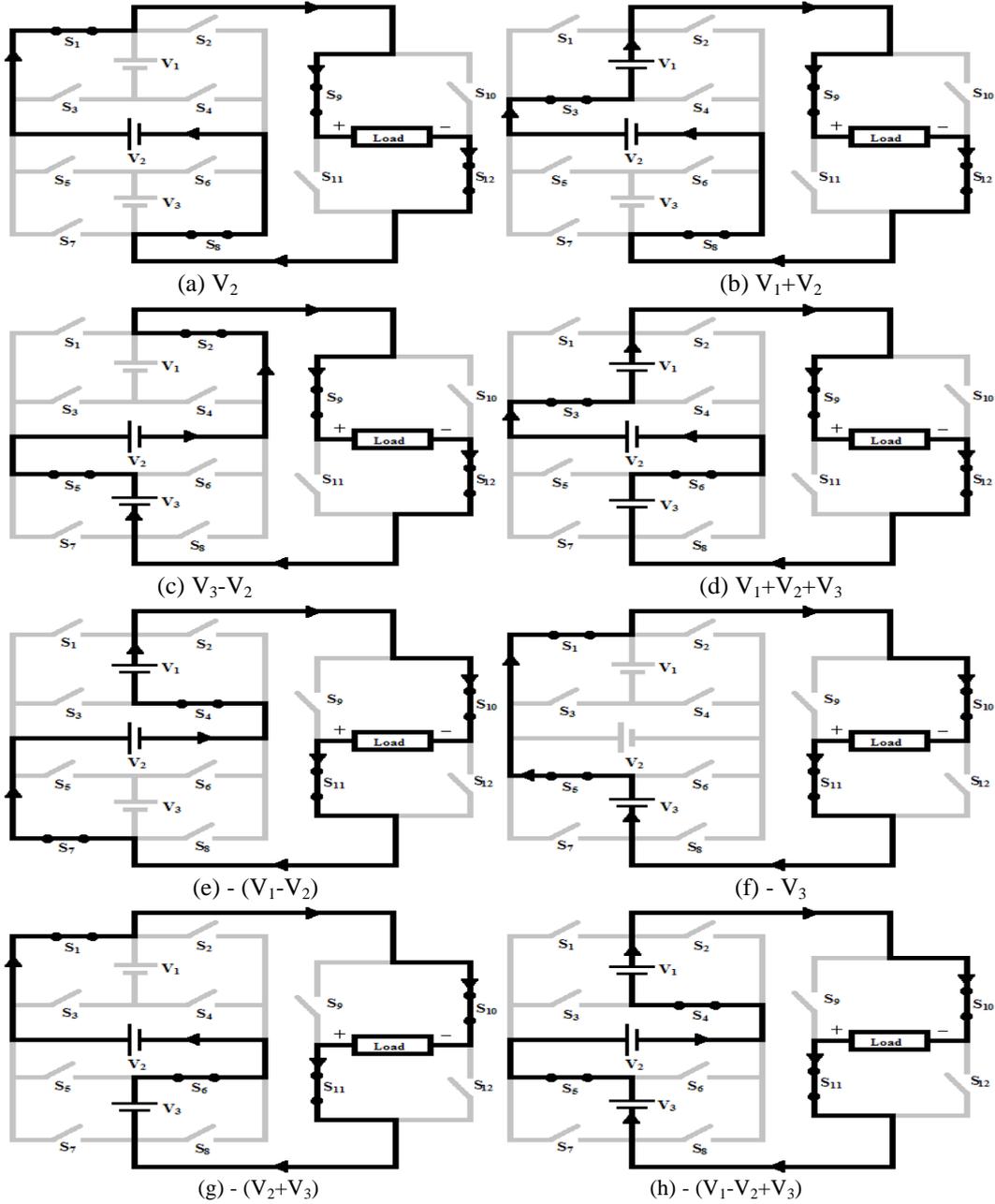(f) $- V_3$

(g) $- (V_2+V_3)$

(h) $- (V_1-V_2+V_3)$

Figure 2. Different output levels of the proposed inverter topology.

The level-7 voltage is obtained when the switches S_1 and S_6 are ON during mode-7. The level-8 voltage is obtained when the switches S_4 and S_5 are ON and the other switches are OFF during mode-8. The voltage level-9 is obtained during mode-9 operation. In this mode, the switches S_4 and S_6 are ON. During mode-10, the level-10 voltage is obtained when the switches S_3 and S_6 are ON and the other switches are OFF. The different output levels of the proposed inverter topology with its current conduction path is shown in Fig. 2. The switching states for different output voltage levels during positive cycle of the proposed multilevel inverter is given in Table 1.

3. COMPARISON

The comparison of the output voltage levels with the number of DC voltage sources, the number of switches and the number of on-state switches for different topologies of multilevel inverter are given in Table 2. For the proposed inverter topology, the ratio of the number of DC sources (N_{dc}) to the number of levels (N) is 0.14 and the ratio of the number of switches (N_S) to the number of levels is 0.57. Therefore, it is clear that the proposed multilevel inverter uses minimum number of switches to achieve fifteen level output voltage. The proposed topology used minimum switching devices and DC voltage sources to generate 21-level output voltage waveform. In addition, the number of on-state switches for the proposed inverter topology is very minimal when compared with other topologies. For the proposed topology, the number of switches in the current conduction path is only 4. This will considerably reduce the switching losses and thereby will increase the efficiency of the proposed inverter topology.

Table 1. Switching States for different output levels.

Mode	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Output Voltage
Mode - 0	0	1	0	0	0	0	0	1	0
Mode - 1	1	0	0	0	0	0	0	1	V_2
Mode - 2	0	0	0	1	0	0	1	0	$V_1 - V_2$
Mode - 3	0	0	1	0	0	0	1	0	V_1
Mode - 4	0	0	1	0	0	0	0	1	$V_1 + V_2$
Mode - 5	0	1	0	0	1	0	0	0	$V_3 - V_2$
Mode - 6	1	0	0	0	1	0	0	0	V_3
Mode - 7	1	0	0	0	0	1	0	0	$V_2 + V_3$
Mode - 8	0	0	0	1	1	0	0	0	$V_1 - V_2 + V_3$
Mode - 9	0	0	0	1	0	1	0	0	$V_1 + V_3$
Mode - 10	0	0	1	0	0	1	0	0	$V_1 + V_2 + V_3$

Table 2. Comparison of different Multilevel Inverters.

Inverter	Number of DC sources (N_{dc})	Number of switches (N_S)	Number of on-state switches	Number of level (N)	Ratio (N_{dc} / N)	Ratio (N_S / N)
Cascaded H-bridge inverter	3	12	6	13	0.23	0.92
Alishah *et al.* 2014	3	7	5	13	0.23	0.54
Babaei *et al.* 2007	3	16	4	13	0.23	1.23
Babaei *et al.* 2012	3	8	5	15	0.20	0.53
Babaei *et al.* 2014	4	12	6	13	0.31	0.92
Babaei *et al.* 2015	4	11	5	9	0.44	1.22
Banaei *et al.* 2013	4	10	6	13	0.31	0.77
Jayabalan *et al.* 2017	3	9	5	13	0.23	0.69
Karasani *et al.* 2016	5	9	4	11	0.45	0.82
Thiyagarajan *et al.* 2017	4	10	4	17	0.23	0.59
Proposed inverter	3	12	4	21	0.14	0.57

4. CALCULATION OF SWITCHING ANGLES

The switching angles play a major role to reduce the of total harmonic distortion (THD) of the output voltage waveform. The different methods of calculating the switching angles for the proposed asymmetrical 21-level inverter are given below Luo *et al.* (2013).

Method - 1

In method-1, the switching angles are distributed averagely over the range 0–90° and are determined by,

$$\theta_j = j\frac{180°}{N} \quad where, i = 1,2,3...,\left(\frac{N-1}{2}\right) \tag{1}$$

Method - 2

In method-2, the switching angles are determined by using the following equation,

$$\theta_j = \frac{1}{2}\sin^{-1}\left(\frac{2j-1}{n-1}\right) where, j = 1,2,...,\left(\frac{n-1}{2}\right) \tag{2}$$

Method - 3

The switching angles for this method are determined by using the following equation,

$$\theta_j = j\frac{180°}{n+1} where, j = 1,2,...,\left(\frac{n-1}{2}\right) \tag{3}$$

Method – 4

The above three methods are capable of arranging the main switching angles where the output waveform is not a sine wave. According to the sine function, a new method to determine the main switching angles were established. The main idea of this method is that when the function value increases to half to the half-height of the output level, the switch angle is set and thus a better output waveform is obtained. In this method, the main switching angles are determined by the formula given below.

$$\theta_j = \sin^{-1}\left(\frac{2j-1}{N-1}\right) \quad where, j = 1,2,3....\left(\frac{N-1}{2}\right) \tag{4}$$

where, N = Number of output levels.

This method gives a better output voltage waveform compared with the other methods as the output waveform is more similar to sine wave. The switching angles corresponding to the period 0 to 90° are called as main switching angles.

The other switching angles are obtained using the following relations:

1. For period 0 to $\pi/2$: $\theta_1, \theta_2, \ldots, \theta_{(n-1)/2}$.

2. For period $\pi/2$ to π : $\theta_{(n+1)/2} \ldots, \theta_{(n-1)} = (\pi - \theta_{(n-1)/2}) \ldots, (\pi - \theta_1)$.

3. For period π to $3\pi/2$: $\theta_n, \ldots, \theta_{3(n-1)/2} = (\pi + \theta_1) \ldots, (\pi + \theta_{(n-1)/2})$.

4. For period $3\pi/2$ to 2π : $\theta_{(3n-1)/2}, \ldots, \theta_{2(n-1)} = (2\pi - \theta_{(n-1)/2}) \ldots, (2\pi - \theta_1)$.

For the proposed 21-level inverter, there are ten main switching angles and these are given in Table 3. The Switching pulses obtained using the different methods are shown in Fig. 3. It is seen that only two main switches were turned on to synthesize the required output voltage at any time.

5. SIMULATION RESULTS

The MATLAB/Simulink simulation results of the proposed asymmetrical 21-level inverter are presented in this section. The proposed inverter consists of three DC voltage sources and eight main switches. The values of the different DC voltage sources are $V_1 = 60V$, $V_2 = 20V$ and $V_3 = 120V$. The magnitude of the voltage sources is selected in the ratio 2:1:3. The maximum voltage obtained as 200 V (*i.e.* $V_1 + V_2 + V_3$). The 21-level output voltage obtained for different switching methods is shown in Fig. 4. It is seen that the output voltage waveform is triangular in shape for method-1 and method-3 as the switching angles are distributed averagely over the range 0–90°. For method-2, the output voltage waveform is trapezoidal in shape. It is also observed that the output voltage waveform is sinusoidal for method-4. The FFT analysis of the 21-level output voltage waveform for different switching methods are shown in Fig. 5. The simulation results show that the harmonic content of the 21-level output voltage waveform for the switching method-4 is less as 3.90% when compared with the other methods. However, it is observed that the fundamental output voltage for the switching method-2 is as high as 240.3 V when compared with the other switching methods. As mentioned in Section 3, method-4 gives a better output voltage waveform compared with the other methods. The comparison of the fundamental output voltage and %THD are given in Table 4. The load current waveform for the different loading conditions is shown in Fig. 6. The comparison of the THD of the load current for different loading conditions is given in Table 5. It is observed that an increase in the inductive load decreases the THD of the current waveform, however, the THD of the voltage waveform remains the same for the proposed inverter topology.
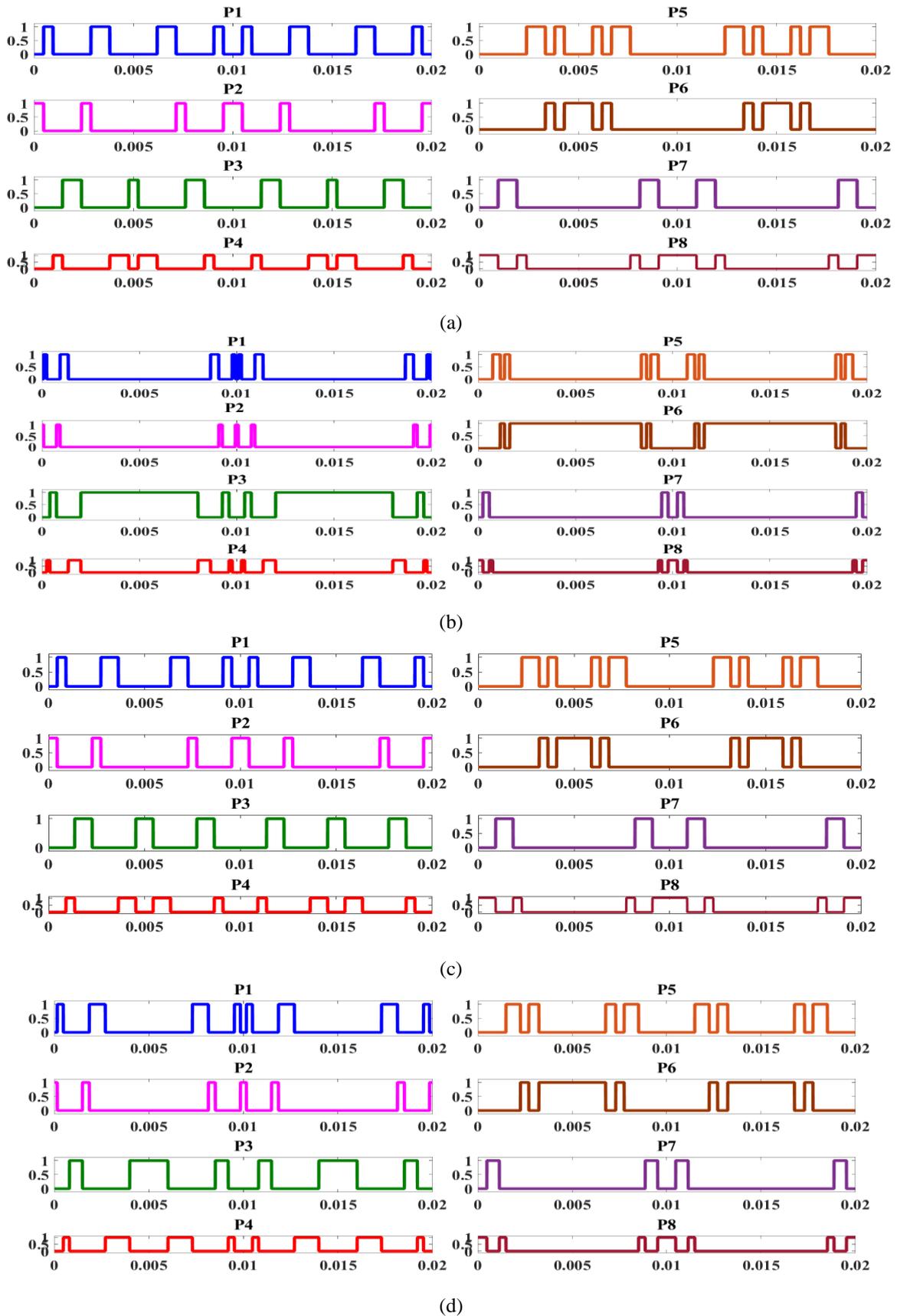
Figure 3. Switching Pulses (a) Method - 1 (b) Method - 2 (c) Method - 3 and (d) Method - 4.

6. CONCLUSION

A new asymmetric type 21-level inverter with a minimum number of switches has been proposed in this paper. The main advantage of this inverter topology is using only three DC voltage sources and eight main switches to achieve 21-level output voltage during the asymmetric mode of operation as compared with other conventional topologies.

The three different methods used to calculate the switching angles are presented and the simulation results are also compared in this paper. The maximum obtained voltage is equal to the sum of the magnitude of the individual voltage. The simulation result shows that the switching angles obtained by method - 4 achieves less THD compared with the other methods. However, method - 2 achieves high fundamental output

Table 3. Switching Angles.

Angle	Main Switching Angles (in degree)			
	Method- 1	Method- 2	Method- 3	Method- 4
θ_1	8.5714	1.433	8.1818	2.866
θ_2	17.1429	4.3135	16.3636	8.6269
θ_3	25.7143	7.2388	24.5455	14.4775
θ_4	34.2857	10.2437	32.7273	20.4873
θ_5	42.8571	13.3718	40.9091	26.7437
θ_6	51.4286	16.6835	49.0909	33.367
θ_7	60.0000	20.2708	57.2727	40.5416
θ_8	68.5714	24.2952	65.4545	48.5904
θ_9	77.1429	29.1058	73.6364	58.2117
θ_{10}	85.7143	35.9026	81.8182	71.8051

Table 4. Comparison of fundamental output voltage and THD.

Method	Fundamental Output Voltage (V)	THD (%)
Method - 1	157.6	16.43
Method - 2	240.3	20.48
Method - 3	165.3	15.74
Method - 4	200.7	3.90

Table 5. Comparison of THD of the current waveform.

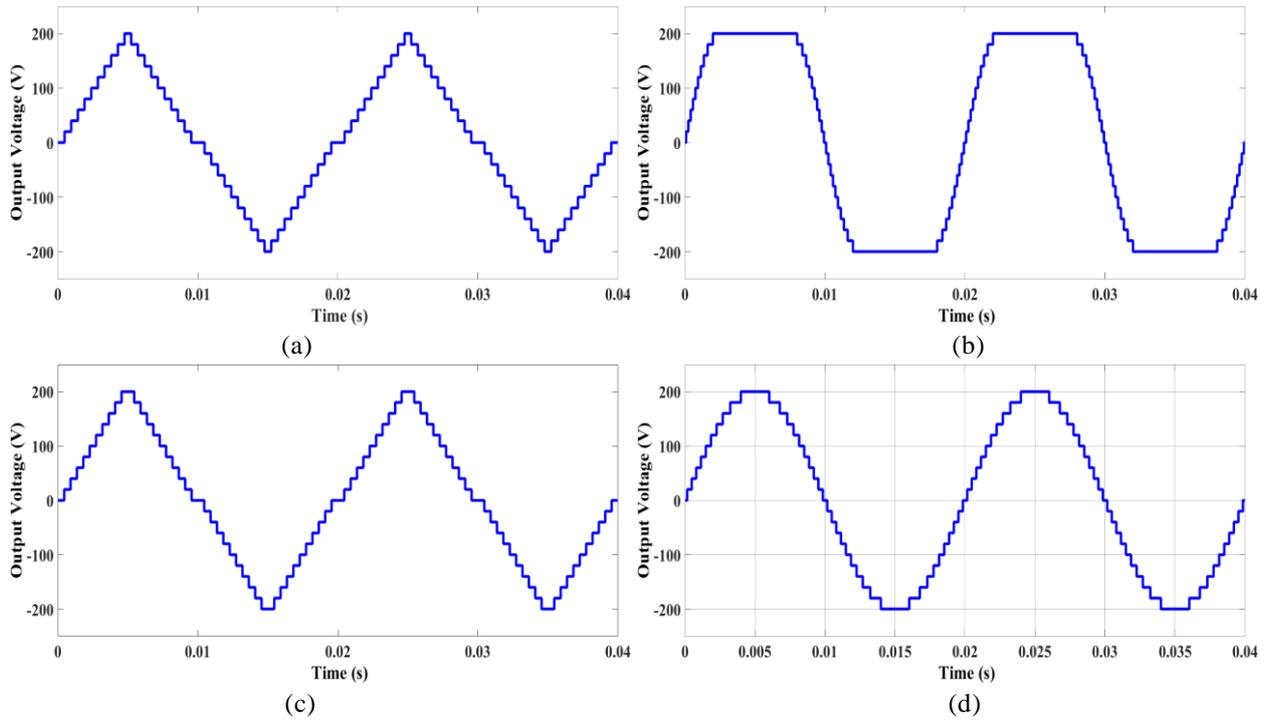| Load	THD (%)			
	Method-1	Method-2	Method-3	Method-4
R=100Ω	16.43	20.48	15.74	3.90
R=100Ω L=5mH	16.10	20.37	15.45	3.05
R=75Ω L=10mH	15.72	20.26	15.12	2.01
R=50Ω L=5mH	15.79	20.37	15.17	2.20

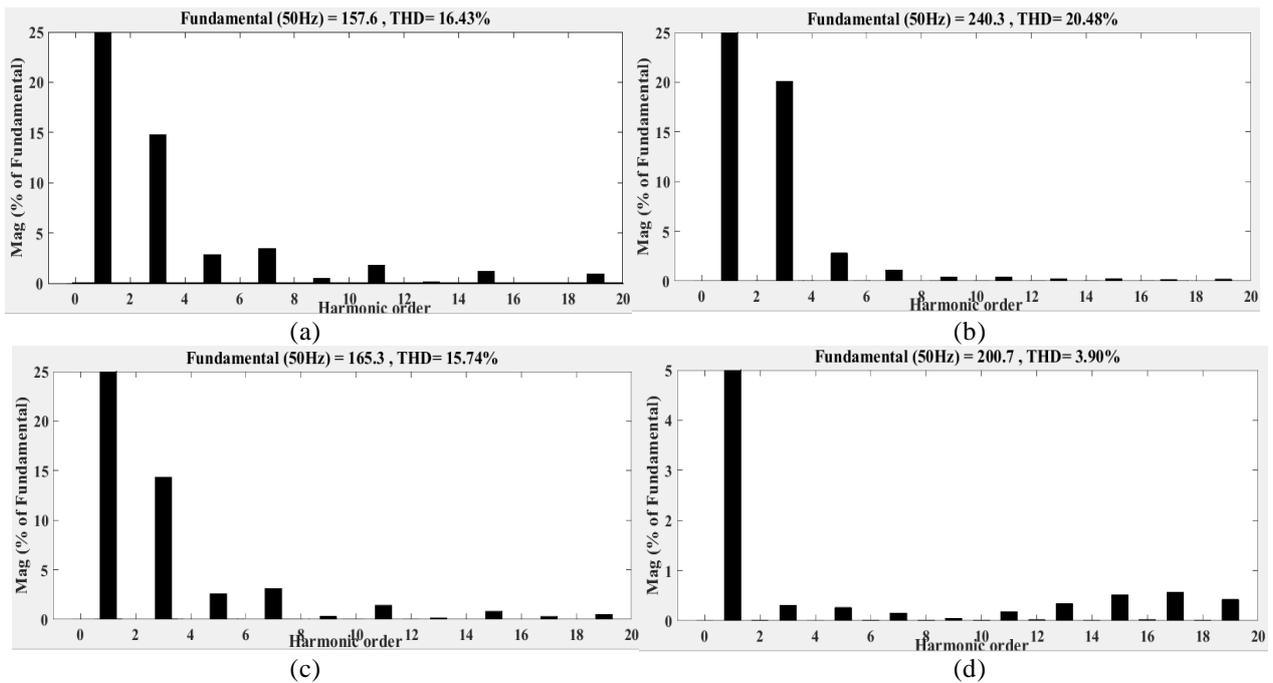**Figure 4**. Output voltage (a) Method - 1 (b) Method - 2 (c) Method – 3 and (d) Method - 4.

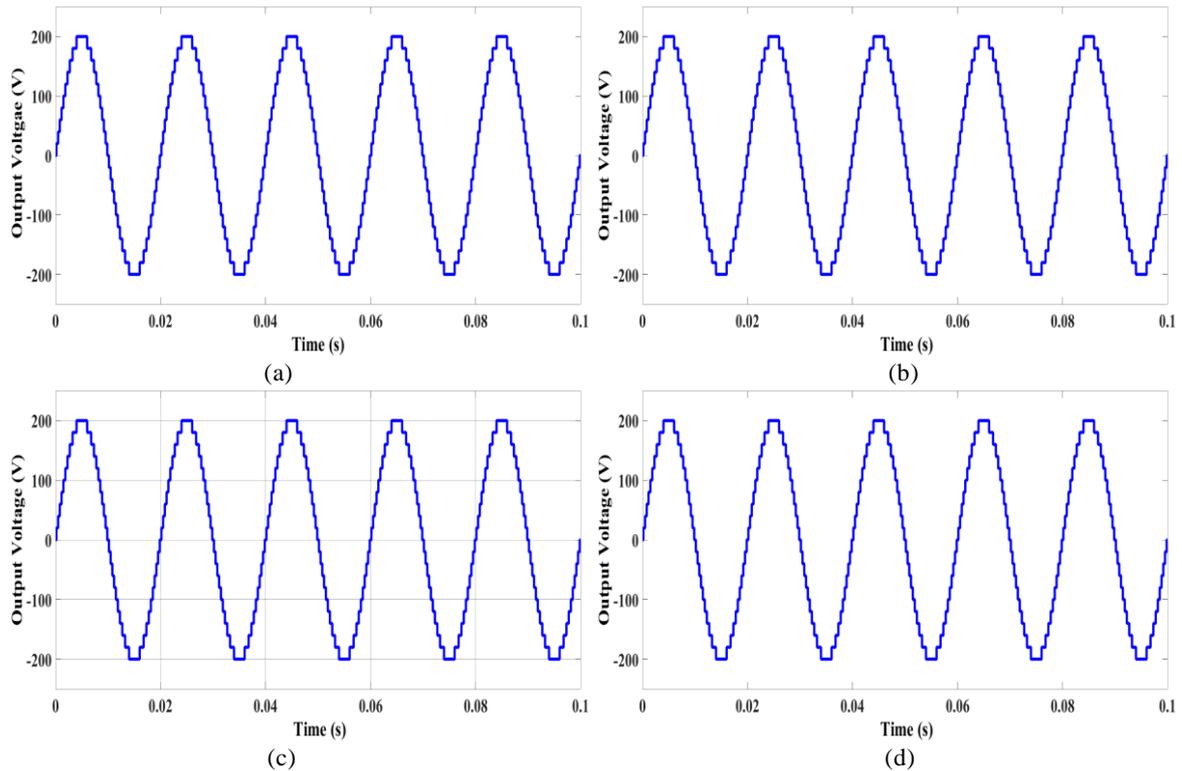**Figure 5**. FFT Analysis (a) Method - 1 (b) Method - 2 (c) Method - 3 and (c) Method - 4.

Figure 6. Output Voltage (a) R=100Ω (b) R=100Ω and L=5mH (c) R=75Ω and L=10mH and (d) R=50Ω and L=5mH.

voltage as compared with the other methods. The major advantage of the proposed 21-level inverter is using a minimum number of switches and hence both the cost and the size of the inverter are reduced.

CONFLICT OF INTEREST

The authors declare no conflicts of interest.

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REFERENCES

Alishah RS, Nazarpour D, Hossein SH, Sabahi M (2014), Design of new single-phase multilevel voltage source inverter. *International Journal of Power Electronics and Drive System* 5(1): 45-55.

Babaei E, Hosseini SH, Gharehpetian GB, Tarafdar Haque M, Sabahi M (2007), Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology. *Electric Power Systems Research* 77: 1073–1085.

Babaei E, Kangarlu MF, Mazgar F (2012), Symmetric and asymmetric multilevel inverter topologies with reduced switching devices. *Electric Power Systems Research* 86:122–130.

Babaei E, Laali S, Alilu S (2014), Cascaded multilevel inverter with series connection of novel H-bridge basic units. *IEEE Transactions on Industrial Electronics* 61(12): 6664-6671.

Babaei E, Laali S, Bayat Z (2015), A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches. *IEEE Transactions on Industrial Electronics* 62(2): 922-929.

Banaei MR, Salary E (2013), Asymmetric cascaded multi-level inverter: A solution to obtain high number of voltage levels. *Journal of Electrical Engineering and Technology* 8(2): 316-325.

Busquets-Monge S, Rocabert J, Rodriguez P, Alepuz S, Bordonau J (2008), Multilevel diode-clamped converter for photovoltaic generators with independent voltage control of each solar array. *IEEE Transactions on Industrial Electronics* 55(7): 2713-2723.

Dargahi S, Babaei E, Eskandari S, Dargahi V, Sabahi M (2014), Flying-capacitor stacked multicell multilevel voltage source inverters: analysis and modelling. *IET Power Electronics* 7(12): 2969-2987.

Farakhor A, Reza Ahrabi R, Ardi H, Najafi RS (2015), Symmetric and asymmetric transformer based cascaded multilevel inverter with minimum number of components. *IET Power Electronics* 8(6): 1052-1060.

Grahame DH, Thomas AL (2003), Pulse width modulation for power converters. *Wiley interscienceInc.*

Islam M, Mekhilef S (2015), H6-type transformerless single-phase inverter for grid-tied photovoltaic system. *IET Power Electronics,* 8(4): 636-644.

Jayabalan M, Jeevarathinam B, Sandirasegarane T (2017), Reduced switch count pulse width modulated multilevel inverter. *IET Power Electronics* 10(1):10-17.

Karasani RR, Borghate VB, Meshram PM, Suryawanshi HM (2016), A modified switched-diode topology for cascaded multilevel inverters. *Journal of Power Electronics* 16(5): 1706-1715.

Li W, Gu Y, Luo H, Cui W, He X, Xia C (2015), Topology review and derivation methodology of single-phase transformerless photovoltaic inverters for leakage current suppression. *IEEE Transactions on Industrial Electronics* 62(7): 4537–4551.

Luo FL,Ye H (2013), Advanced DC/AC inverters. *CRC Press* LLC.

Meynard TA (2002), Multicell converters: derived topologies. *IEEE Transactions on Industrial Electronics* 49(5): 978-987.

Nabae A, Takahashi I, Akagi H (1981), A new neutral-point-clamped PWM inverter. *IEEE Transactions on Industry Applications* 17(5): 518-523.

Prabaharan N, Palanisamy K (2015), Investigation of single phase reduced switch count asymmetric multilevel inverter using advanced pulse width modulation technique. *International Journal of Renewable Energy Research* 5(3): 879-890.

Rahim NA, Selvaraj J (2010), Multistring five-level inverter with novel PWM control scheme for PV application. *IEEE Transactions on Industrial Electronics*, 57(6): 2111–2123.

Ramani K, Sathik MA, Sivakumar S (2015) A new symmetric multilevel inverter topology using single and double source sub-multilevel inverters. *Journal of power electrronics* 15(1): 96-105.

Sadigh AK, Hosseini SH, Sabahi M, Gharehpetian G.B. (2010), Double flying capacitor multicell converter based on modified phase-shifted pulsewidth modulation. *IEEE Transactions on Power Electronics* 25(6): 1517-1526.

Samadaei E, Gholamian SA, Sheikholeslami A, Adabi J (2016), An envelope type (E-Type) module: asymmetric multilevel inverters with reduced components. *IEEE Transactions on Industrial Electronics* 63(11): 7148-7156.

Thiyagarajan V, Somasundaram P (2016), Performance analysis of photovoltaic array with H5 inverter under partial shading conditions. *International Journal of Innovation and Scientific Research* 22(1): 164-177.

Thiyagarajan V, Somasundaram P (2017), Modeling and analysis of novel multilevel inverter topology with minimum number of switching components. *CMES: Computer Modeling in Engineering and Sciences* 113(4): 461-473.

Toupchi Khosroshahi M (2014), Crisscross cascade multilevel inverter with reduction in number of components. *IET Power Electronics* 7(12): 2914-2924

Vafakhah B, Salmon J, Knight AM (2010), A new space-vector PWM with optimal switching selection for multilevel coupled inductor inverters. *IEEE Transactions on Industrial Electronics* 57(7): 2354-2364.

Zhang F, Yan Y (2009), Selective harmonic elimination PWM control scheme on a three-phase four-leg voltage source inverter. *IEEE Transactions on Power Electronics* 24(7): 1682-1689.